

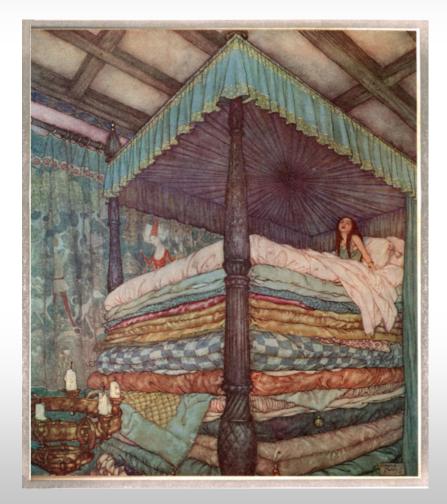
## Information Security – Theory vs. Reality

#### 0368-4474, Winter 2015-2016

#### Lecture 2: Architectural side-channels (2/2)

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# Course agenda





# Architectural side-channel attacks (cont.)

- Target outermost cache, shared between all CPU cores (typically L3)
- RSA key extraction from GnuPG 1.4.13
- Target specific memory block (instead of cache set)
- Exploits memory deduplication (contentbased page sharing)
  - Common code, libraries, data across VMs
  - Supposedly safe (nominally, no new information flow)

#### L3 flush+reload attack (cont.)

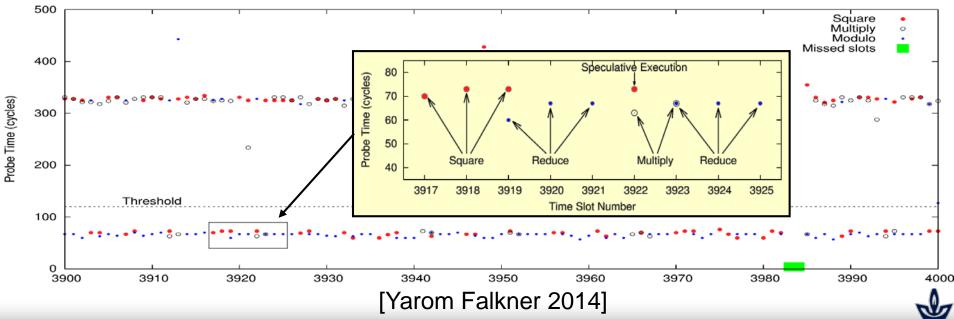
To measure a memory block *b*, the attacker:

- Achieve page sharing of *b* with victim
- Flush block b using x86 clflush instruction
  - Flushes block from all cache levels
  - Normally used for synchronization / performance
- Wait until victim runs
- Measure time to read the block *b* 
  - Fast  $\rightarrow$  victim accessed b
  - Slow victim did not access b

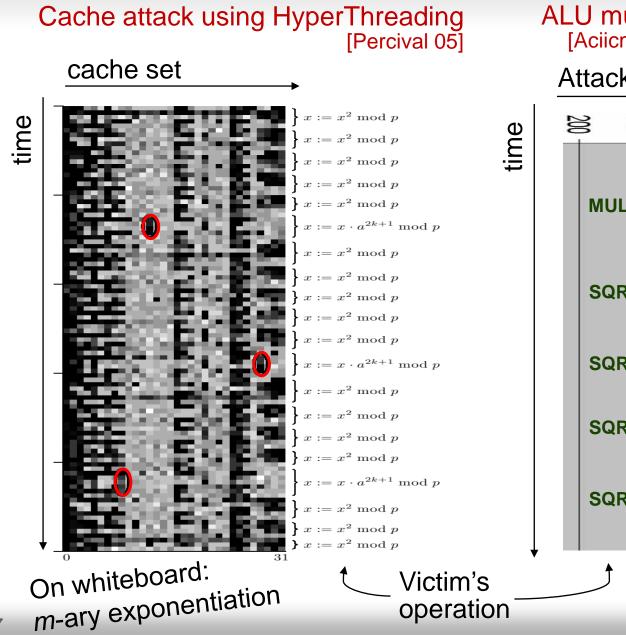


#### L3 flush+reload attack on GnuPG's RSA

- GnuPG 1.4.13 uses square-and-multiply exponentiation.
- Repeatedly measure blocks in the code of the square, multiply and modulo routines.
- Read out the bits from the sequence during a single RSA decryption
  - multiply between adjacent square  $\rightarrow$  key bit is 1
  - No multiply between adjacent square  $\rightarrow$  key bit is 0

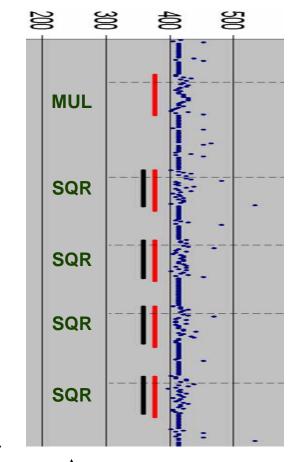


#### Other attacks on RSA



#### ALU multiplier attack [Aciicmez Seifert 2007]

#### Attacker's MUL time





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### Other architectural attacks

(Whiteboard discussion)

Covert channels     Hardware, assisted	[Hu '91, '92]
<ul> <li>Hardware-assisted         <ul> <li>Power trace</li> </ul> </li> </ul>	[Page '02]
<ul> <li>Timing attacks via internal collisions</li> </ul>	
	o Tsujihara Minematsu Miyuachi '02] oo Saito Suzaki Shigeri Miyauchi '03]
<ul> <li>Model-less timing attacks</li> </ul>	[Bernstein '04]
• RSA	[Percival '05]
<ul> <li>Exploiting the scheduler</li> </ul>	[Neve Seifrert '07]
<ul> <li>Improve temporal resolution by causing victim to get tiny time slice</li> </ul>	
Instruction cache	Aciicmez '07]
<ul> <li>Exploits difference between code paths</li> </ul>	
<ul> <li>Attacks are analogous to data cache attack</li> </ul>	
Branch prediction	[Aciicmez Schindler Koc '06–'07]
<ul> <li>Exploits difference in choice of code path</li> </ul>	
<ul> <li>BP state is a shared resource</li> </ul>	
ALU resources	[Aciicmez Seifert '07]
<ul> <li>Exploits contention for the multiplication units</li> </ul>	
<ul> <li>Many followups</li> </ul>	

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#### Mitigation

#### (classroom discussion)