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1 -----
2 -- Main Entity for Ultra37K-EVB
3 -- Written by Dr. Eli Flaxer
4 -----
5 entity Main is
6     port (
7         IO1      : inout std_logic;
8         IO2      : inout std_logic;
9         A0       : out   std_logic;
10        WR       : out   std_logic;
11        PUSH     : in    std_logic;
12        LEADS    : out   std_logic_vector(7 downto 0);
13        SEGA     : out   std_logic_vector(7 downto 0);
14        SEGB     : out   std_logic_vector(7 downto 0);
15        DATA    : out   std_logic_vector(7 downto 0);
16        SW       : in    std_logic_vector(7 downto 0);
17        RESET    : in    std_logic;
18        CLK      : in    std_logic
19    );
20 end Main;
21
22 architecture Test of Main is
23 -----
```