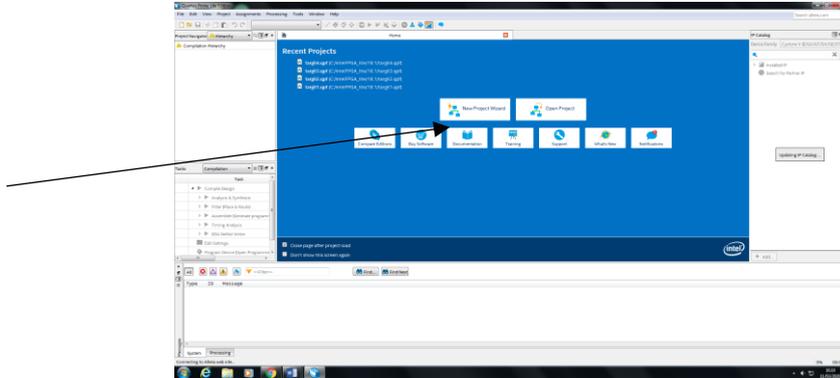


Working with Quartus

Open Quartus

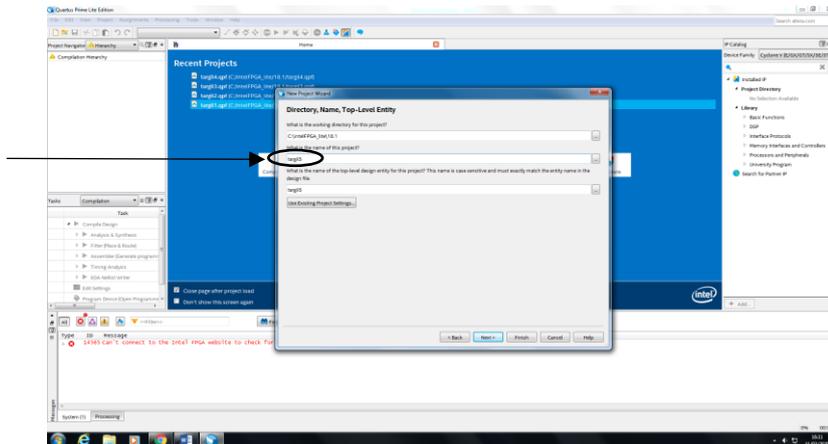
1. Define the project

File -> new project wizard or in the gui



Click next

Give the project a name



Click next

Select empty project

Click next

Add files: click next

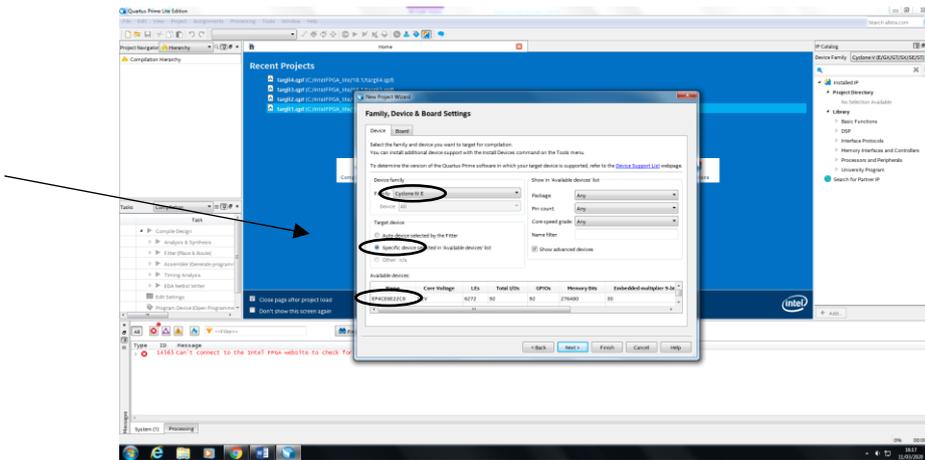
Family, Device & Settings:

Select family: cyclone IV E

Mark specific device selected in "available devices" list

In available devices list choose: EP4CE6E22C8

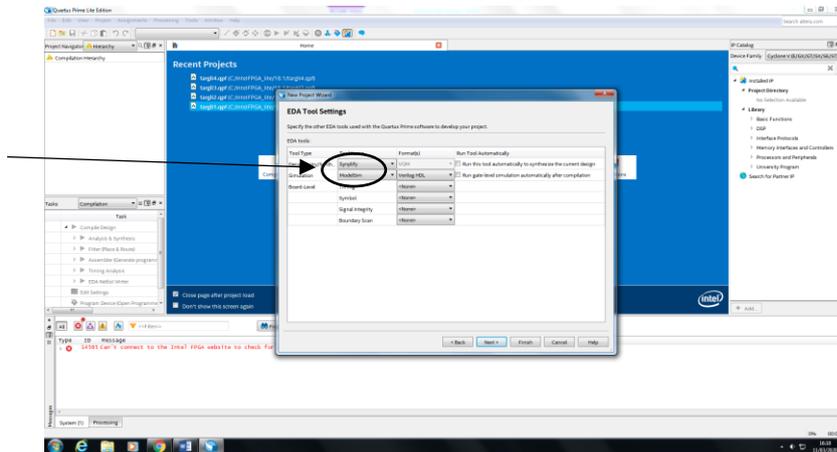
Next



EDA Tool Setting:

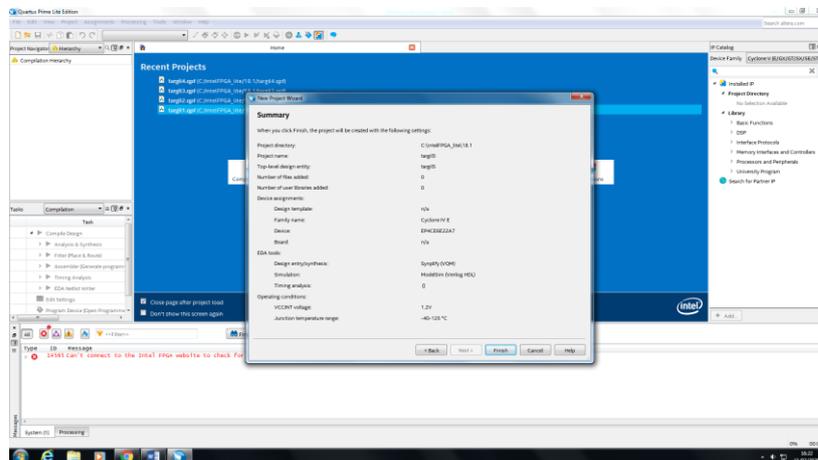
Select in design entry/synthesis: synplify

Select in Simulation: modelsim



Next

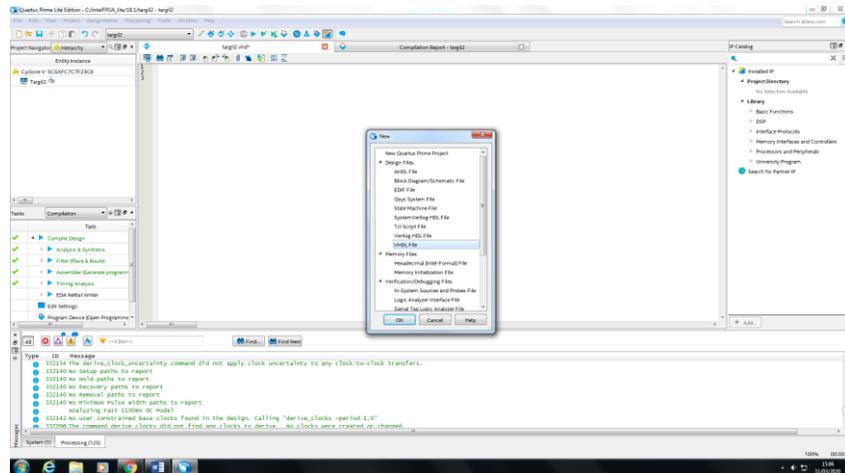
A summary of the project's definitions



Finish

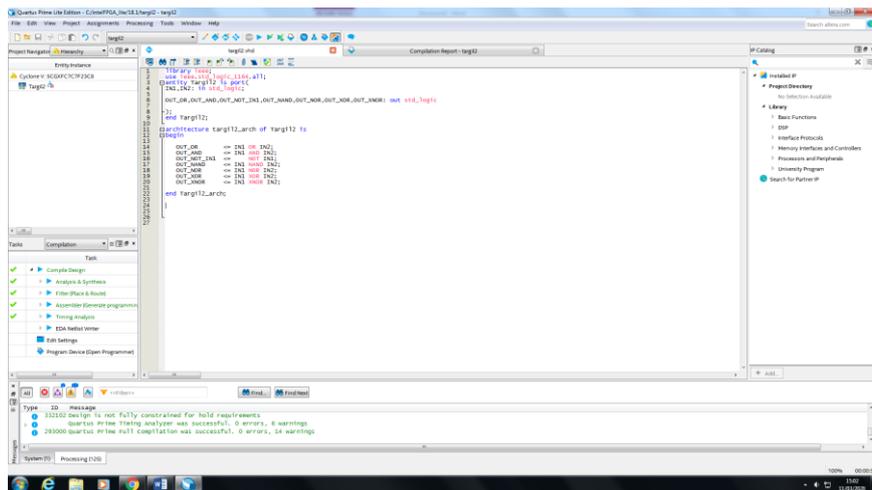
2. Write the VHDL file

File -> new -> design files -> vhd file -> OK

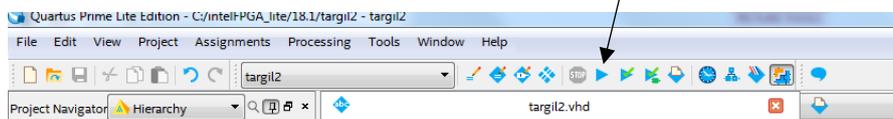


Write the VHDL code and save as *.vhd file

The name of the file should be same as the name of the entity

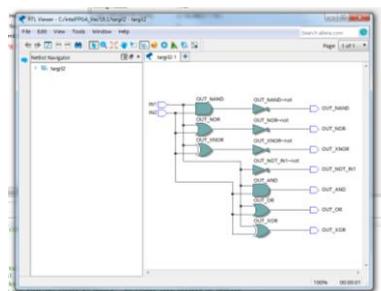


Run compilation by pushing the blue triangle



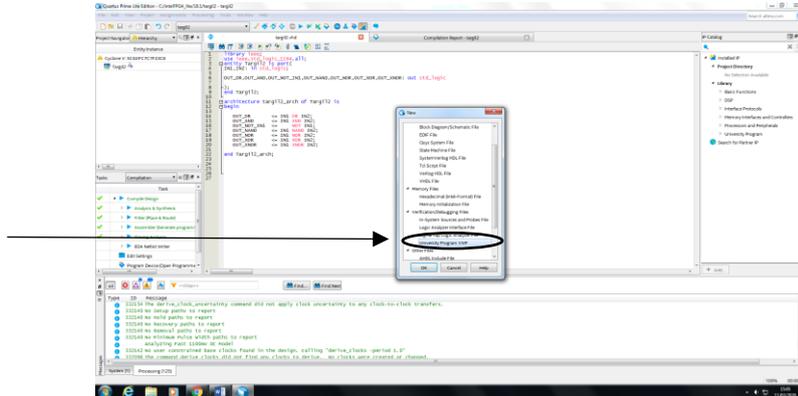
To view the design after synthesis:

Tools -> netlist viewer -> RTL viewer

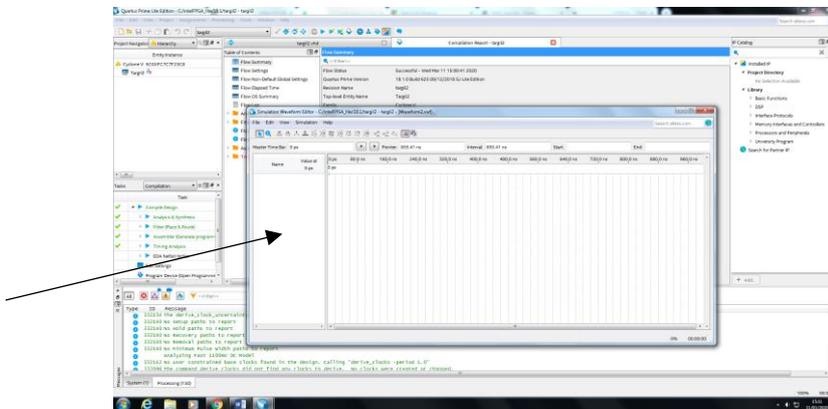


3. Driving inputs

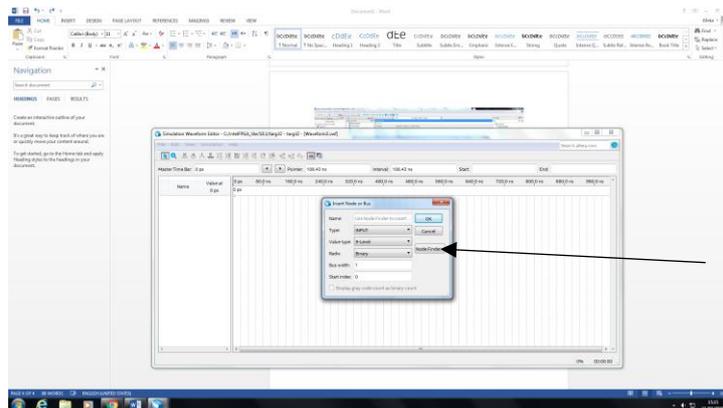
File -> new -> verification/debugging files -> university program VWF -> OK



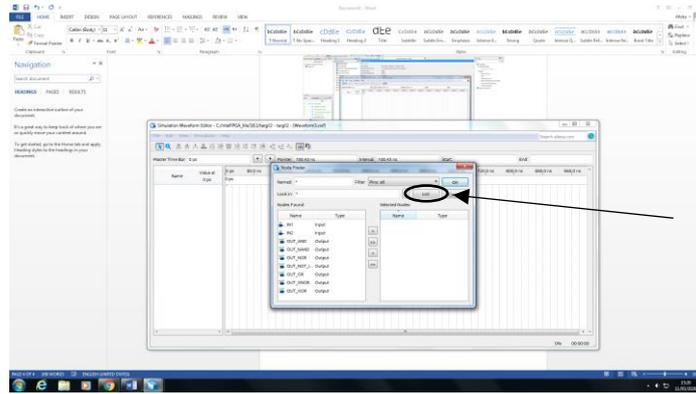
Click the right button in the name area. Select "Insert Node or Bus"



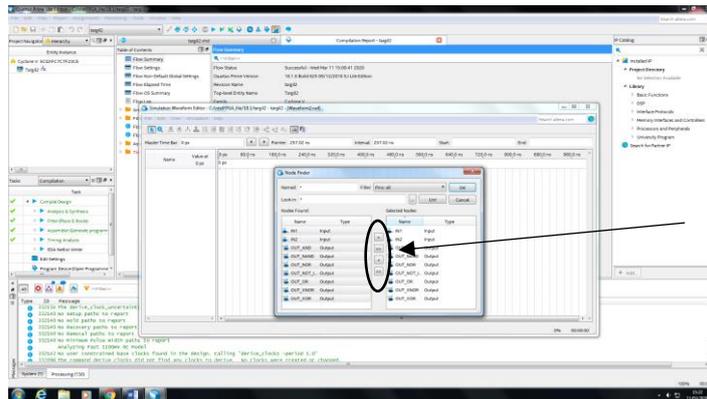
Push "Node Finder"



Push "List". All inputs & outputs will be displayed



Move the inputs and outputs to the right window by pressing the arrow

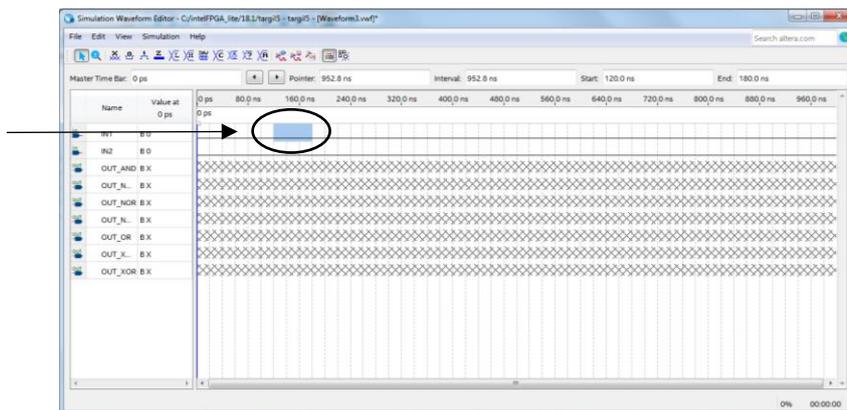


OK

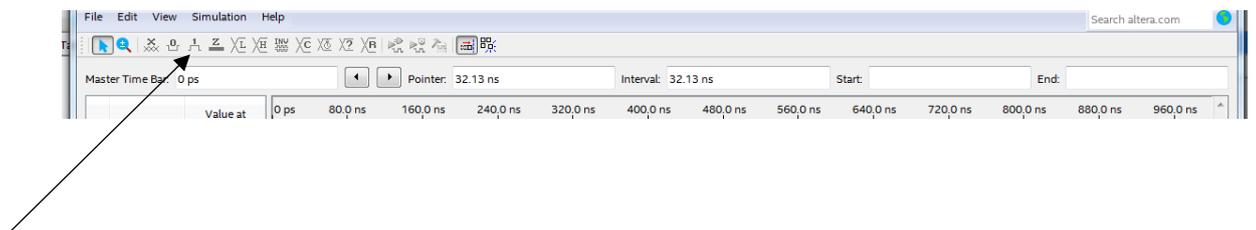
OK

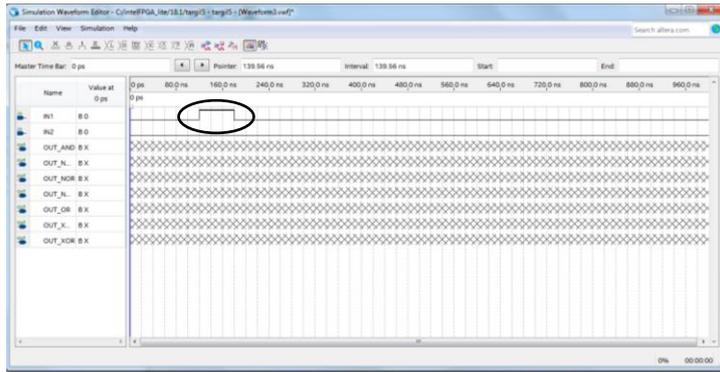
Generate stimuli:

Option 1: Mark the cubes you would like to change

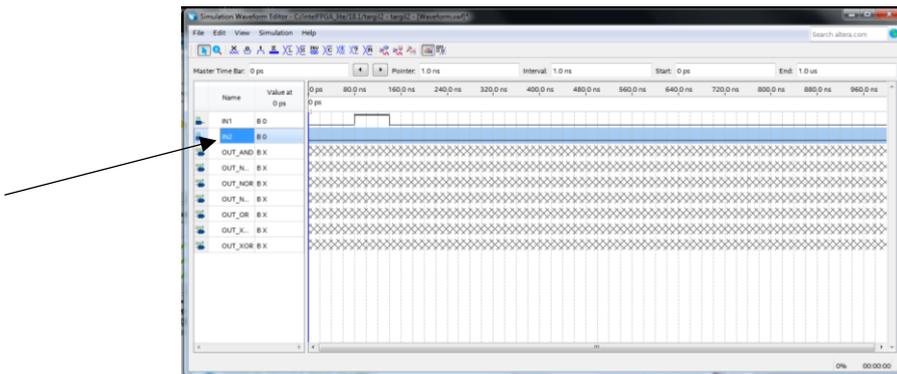


Press the "1"

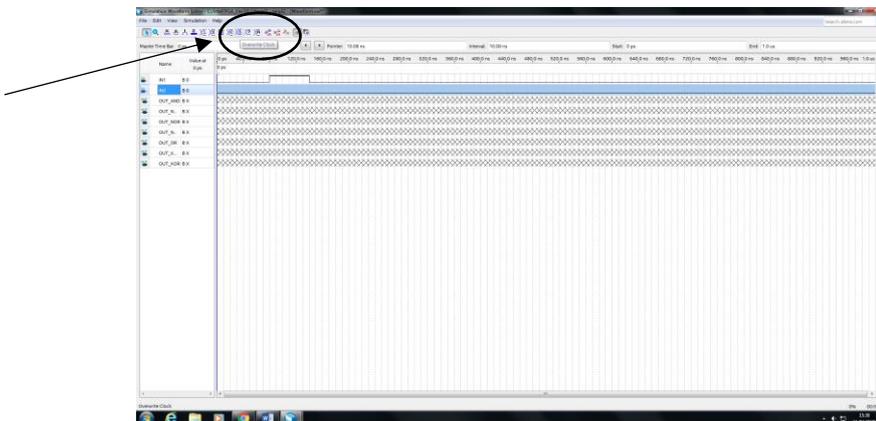




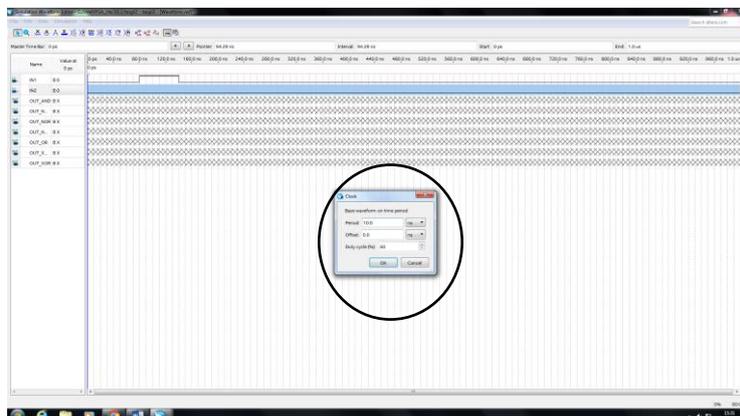
Option 2: press the signal name



Press the "overwrite clock"

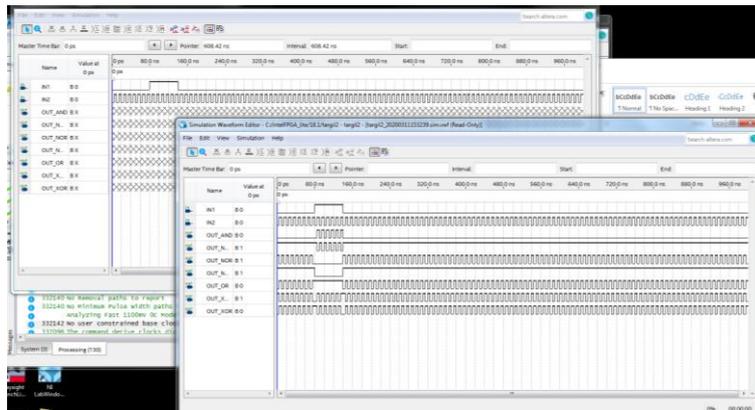


Define frequency.



4. Running simulation

Simulation -> run functional simulation



Simulation -> run timing simulation

You can see there is a delay between the inputs and the outputs

