Quartus prime lite + ModelSim לינק להורדת

https://fpgasoftware.intel.com/19.1/?edition=lite

Download Center for FPGAs

| Design Software | Quartus Primo Lito Edition | |
|-----------------------|---|--|
| Embedded Software | Palassa data Sentember 2010 | |
| Archives | Latest Release: v19.1 | Intel' Quartus' Prime |
| Licensing | | Design Software |
| Programming Software | Select edition: Lite 🗸 | |
| Drivers | Select release: 19.1 🗸 | |
| Board System Design | | |
| Board Layout and Test | Operating System 👔 🔍 Windows 🔿 🐧 Linux | |
| Legacy Software | | |
| | Very first software up to classe and follow the <u>rectinitian econfine trought</u> to help improve security. Additional security updates are planned and will be provided as they become available. Users should promptly install the latest version upon release. To use the Quartus Prime Lite Edition Design Software, Version 19.1 on Windows, you must download and install the patch available in this <u>KDB Solution</u>. OS Support and IP support have changed in this release. Refer to the <u>Release Notes</u> for details. The Quartus Prime Lite Edition Design Software, Version 19.1 supports the following device families: Arria II. (536.5MB), Cyclone 10 LP. (293.5MB), Cyclone IV. (516.3MB), Cyclone V. (1434.3MB), MAX II, MAX V. (13.1MB), and MAX 10 FPGA. (343.3MB). | |
| | Combined Eiler Individual Eiler Additional Sc | fhunen |
| | Combined Files Individual Files Additional Software | |
| | Download and install instructions: Vere | |
| | Read Intel FPGA Software v19.1 Installation FAQ | |
| | Quick Start Guide | |
| | | |
| | Quartus Prime Lite Edition (Free) | |
| | Quartus Prime (includes Nios II EDS) | |
| | Size: 1.5 GB MD5: C64B01C9F5DE3E14724F ** Nios II EDS on Windows requires Ubuntu 18.04 LTS requires a manual Installation. ** Nios II EDS requires you to install an Eclipse IDE ma | IOCA046E56A3E S on Windows Subsystem for Linux (WSL), which anually. |
| | ModelSim-Intel FPGA Edition (includes Star Size: 968.2 MB MD5: C094C7B72139545F77 | rter Edition) 7D93DB0F750594C |

<u>עבודה ב Quartus</u>

New Project Wizard \rightarrow choose a working directory and a name for the project \rightarrow Finish

Creating VHDL file: File \rightarrow New \rightarrow VHDL File

Same For the Testbench: File \rightarrow New \rightarrow VHDL File (choose a different name and save at the same directory)

(CTRL+K to compile)