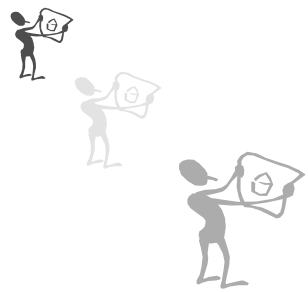
Chapter 4

Memory

Process Control

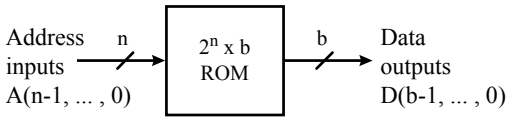
Outline

- **Read-Only Memory (ROM)**
  - **Internal Structure**
  - Control and Timing
- Static RAM (SRAM)
  - Internal Structure
  - Control and Timing
- Dynamic RAM (DRAM)
  - Internal Structure
  - Control and Timing



Read-Only Memory (ROM)

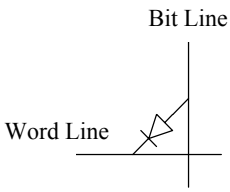
- A combinational circuit with n inputs and b outputs:



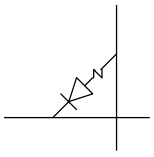
- Programmable — values determined by user
- Nonvolatile — contents retained without power

Types Of ROMs (1)

- Mask ROM
  - Connections made by the semiconductor vendor
  - Expensive setup cost
  - Several weeks for delivery
  - High volume only
  - Bipolar or MOS technology

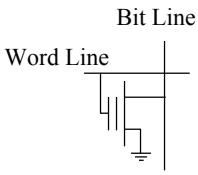


- PROM
  - Programmable ROM
  - Connections made by equipment manufacturer
  - Vaporize (blow) fusible links with PROM programmer using high voltage/current pulses
  - Bipolar technology
  - One-time programmable

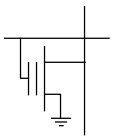


Types of ROMs (2)

- EPROM
  - Erasable Programmable ROM
  - Charge trapped on extra “floating gate” of MOS transistors
  - Exposure to UV light removes charge
    - 10-20 minutes
    - Quartz Lid = expensive package
  - Limited number of erasures (10-100)



- EEPROM (E^2ROM)
  - Electrically Erasable ROM
  - Floating gates charged/discharged electrically
  - Not RAM! (relatively slow charge/discharge)
  - limited number of charge/discharge cycles (10,000)

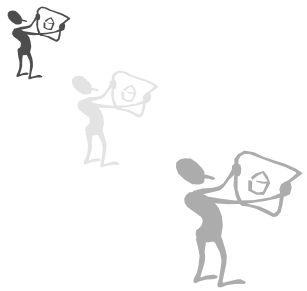


Types of ROMs (3)

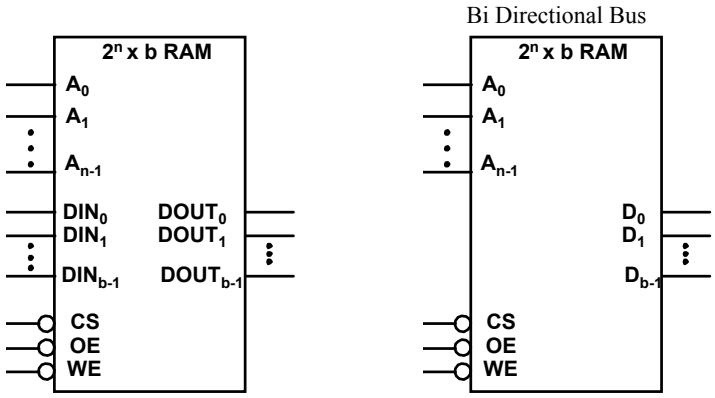
- Flash Memory
  - Electronically erasable in blocks
  - 100,000 erase cycles
  - Simpler and denser than EEPROM

Outline

- Read-Only Memory (ROM)
  - Internal Structure
  - **Control and Timing**
- ➡ Static RAM (SRAM)
  - Internal Structure
  - Control and Timing
- Dynamic RAM (DRAM)
  - Internal Structure
  - Control and Timing

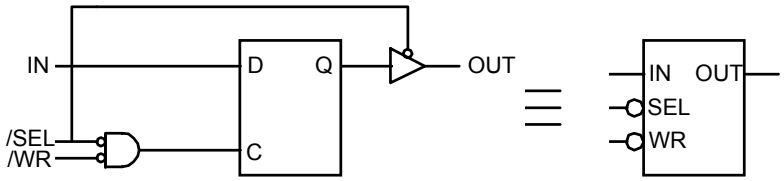


Basic Structure of SRAM



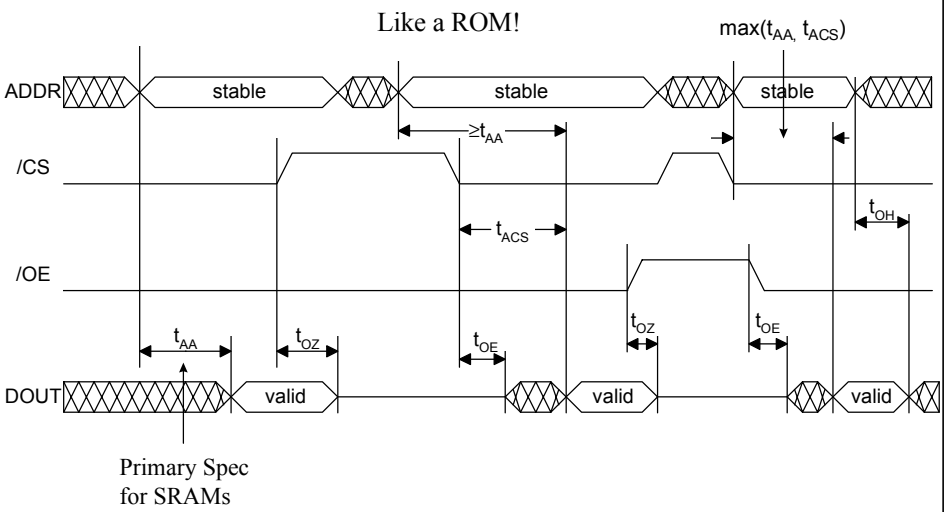
- Address/Control/Data Out lines like a ROM (Reading)
  + Write Enable (WE) and Data In (DIN) (Writing)

One Bit of SRAM

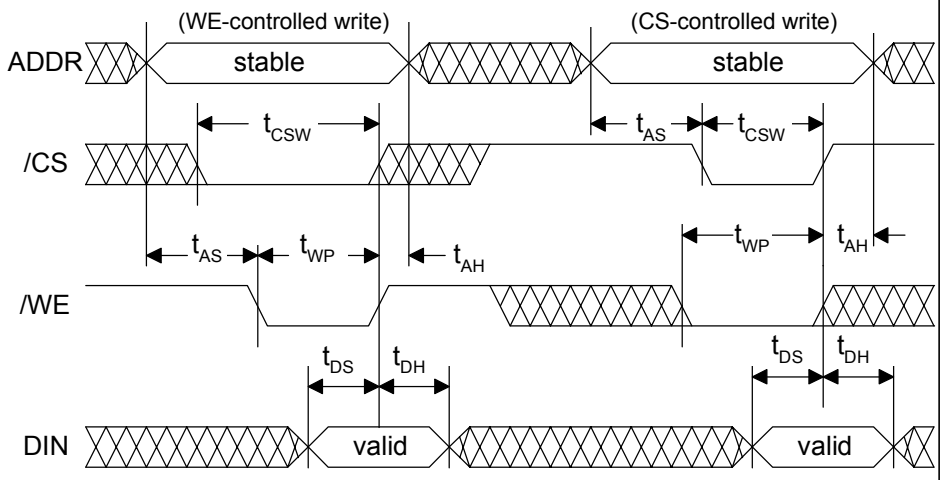


- SEL and WR asserted → IN data stored in D-latch (Write)
- SEL only asserted → D-latch output enabled (Read)
- SEL not asserted → No operation

READ Timing (SRAM)



WRITE Timing (SRAM)



RAM Summary

SRAM:

- Fast
- Simple Interface
- Moderate bit density (4 gates → 4 to 6 transistors)
- Moderate cost/bit

} Small systems or very fast applications (cache memory)

DRAM (Dynamic RAM):

- moderate speed
- complex interface
- High bit density (1 transistor cell)
- Low cost/bit

} Large Memories: PC's Mainframes