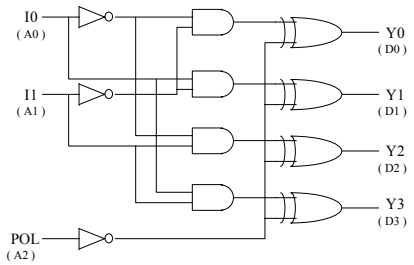
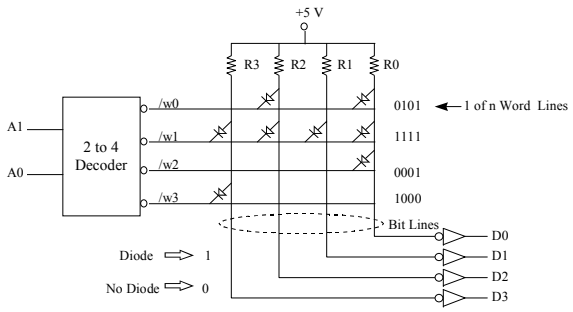
Equivalent Decoder in Discrete Logic

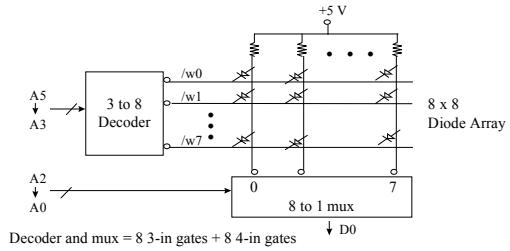


Internal Structure of 4×4 Diode ROM

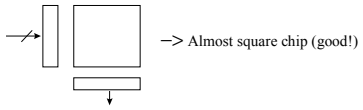


Why use diodes?
Why not replace them with wires?

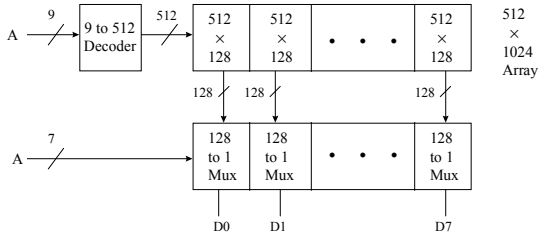
64 x 1 ROM with 2-Dimensional Decoding



Decoder and mux = 8 3-in gates + 8 4-in gates

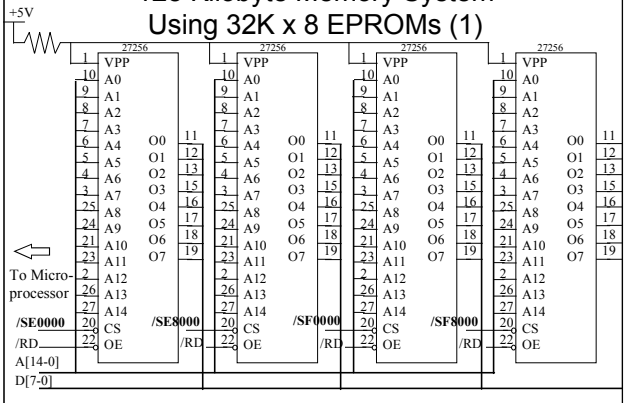


64K x 8 ROM with 2-D Decoding

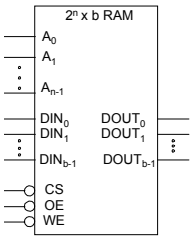


Is this a square chip?

128 Kilobyte Memory System Using 32K x 8 EPROMs (1)

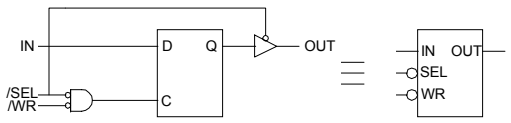


Basic Structure of SRAM

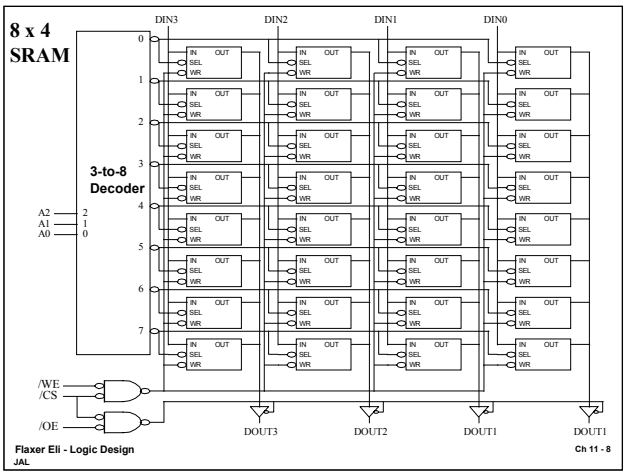


- Address/Control/Data Out lines like a ROM (Reading)
  + Write Enable (WE) and Data In (DIN) (Writing)

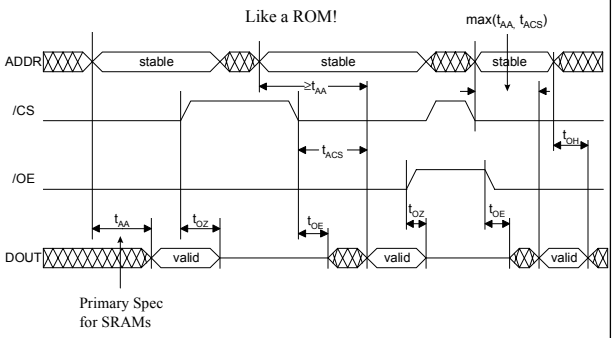
One Bit of SRAM



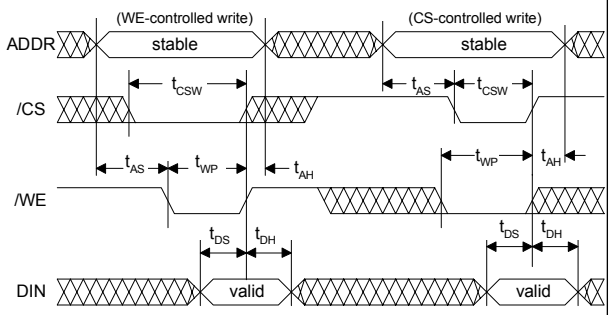
- SEL and WR asserted → IN data stored in D-latch (Write)
- SEL only asserted → D-latch output enabled (Read)
- SEL not asserted → No operation



READ Timing (SRAM)

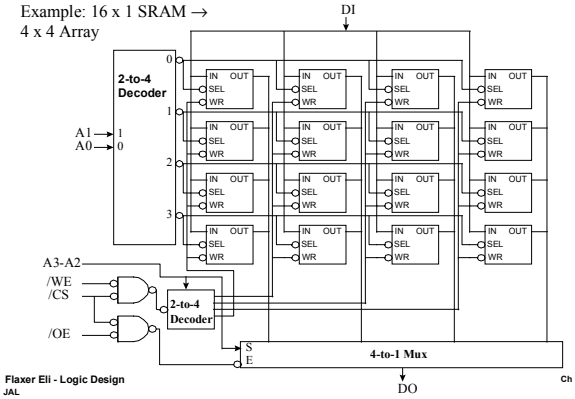


WRITE Timing (SRAM)



Physical SRAM Array Should Be Square

Example: 16 x 1 SRAM → 4 x 4 Array



SRAM with Bidirectional Data Bus