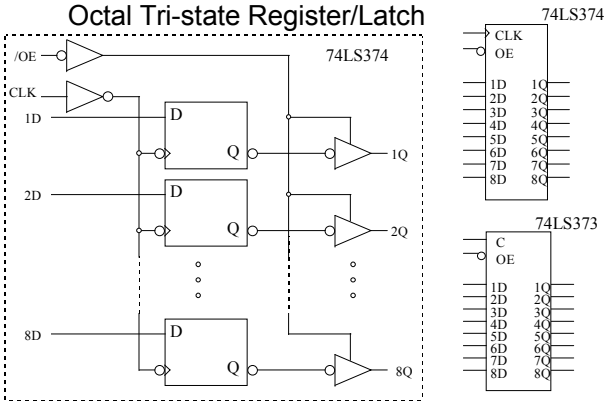
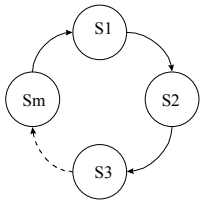
Octal Tri-state Register/Latch



Counters

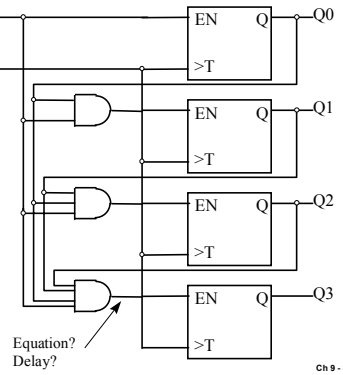
- Clocked sequential circuit with single-cycle state diagram
  - Modulo-m counter = divide-by-m counter



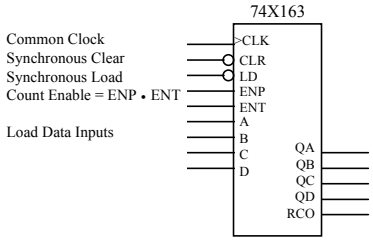
- Most Common:
  n-bit binary counter, where $m = 2^n \rightarrow$ n flip-flops, counts 0 … 2^n-1

Synchronous Parallel Counter

- Single-level enable logic per flip-flop
- Fastest and most complex type of counter
- Requires $\Delta t < T_{CLK}$
- All outputs change simultaneously t_{CQ} after CLK ↑



74163 4-bit Synchronous Parallel Counter

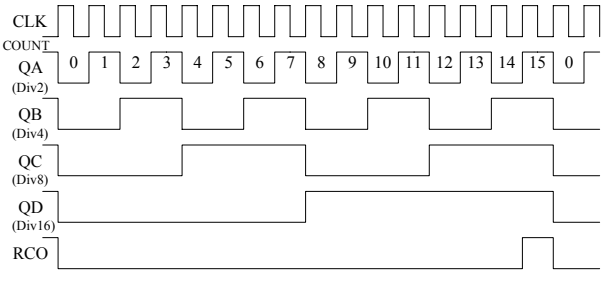


(74161 is the same, but with an asynchronous clear)

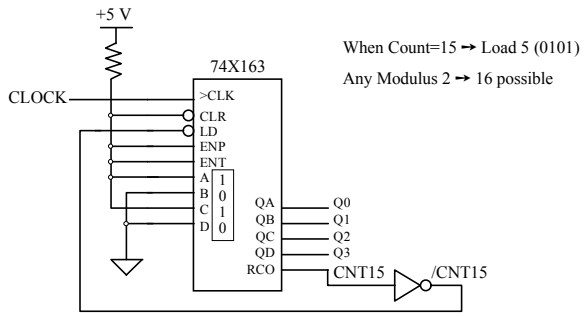
74163 State Table

Inputs					Current State				Next State			
/CLR	/LD	ENT	ENP		QD	QC	QB	QA	QD*	QC*	QB*	QA*
0	X	X	X	Clear	X	X	X	X	0	0	0	0
1	0	X	X	Load	X	X	X	X	D	C	B	A
1	1	0	X	Hold	X	X	X	X	QD	QC	QB	QA
1	1	1	0	Hold	X	X	X	X	QD	QC	QB	QA
1	1	1	1	Count	0	0	0	0	0	0	0	1
1	1	1	1		0	0	0	1	0	0	1	0
1	1	1	1		0	0	1	0	0	0	1	1
1	1	1	1		0	0	1	1	0	1	0	0
1	1	1	1		0	1	0	0	0	1	0	1
1	1	1	1		0	1	0	1	0	1	1	0
1	1	1	1		0	1	1	0	0	1	1	1
1	1	1	1		0	1	1	1	1	0	0	0
1	1	1	1		1	0	0	0	1	0	0	1
1	1	1	1		1	0	0	1	1	0	1	0
1	1	1	1		1	0	1	0	1	0	1	1
1	1	1	1		1	0	1	1	1	1	0	0
1	1	1	1		1	1	0	0	1	1	0	1
1	1	1	1		1	1	0	1	1	1	1	0
1	1	1	1		1	1	1	0	1	1	1	1
1	1	1	1		1	1	1	1	0	0	0	0

Free-Running Modulo-16 Counter Timing Diagram



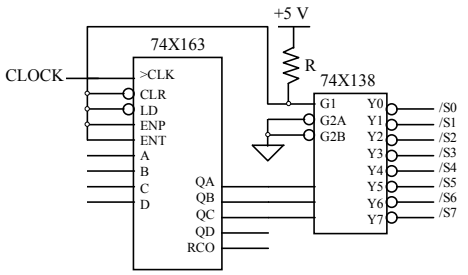
Modulo-11 Counter [5,6, …, 15, 5, 6, ...]



When Count=15 ➙ Load 5 (0101)

Any Modulus 2 ➙ 16 possible

Decoded Modulo-8 Counter

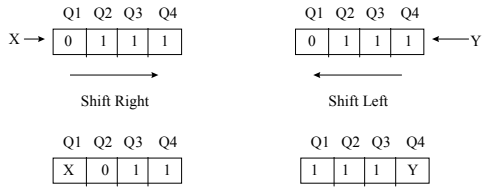


Only one output true per state

Better Solution: Ring Counter
Less logic, simpler to understand

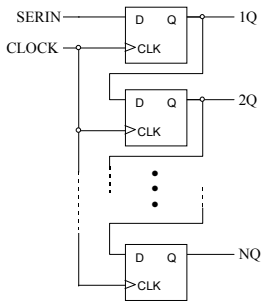
Shift Registers

- Multi-bit register that moves data “sideways” left/right (1 bit/clock)



⇒ Often used to rearrange bits or Multiply/Divide by 2

Serial In, Parallel Out (SIPO) Shift register

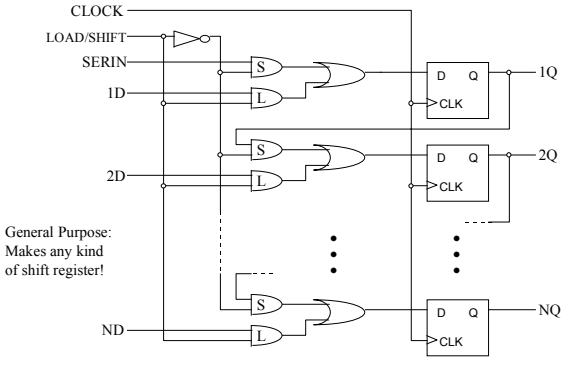


Serial to Parallel Converter

4-bit shift register example:

serin:	1 0 1 1 0 0 1 1 1 0
1Q:	- 1 0 1 1 0 0 1 1 1
2Q:	- - 1 0 1 1 0 0 1 1
3Q:	- - - 1 0 1 1 0 0 1
4Q:	- - - - 1 0 1 1 0 0
clock:	↑ ↑ ↑ ↑ ↑ ↑ ↑ ↑ ↑ ↑

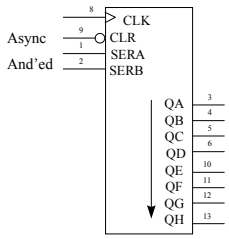
Parallel In, Parallel Out (PIPO) Shift Register



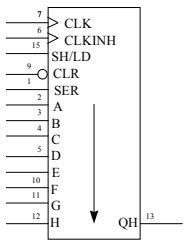
General Purpose:
Makes any kind of shift register!

MSI Shift Registers

Octal (8-bit) SIPO

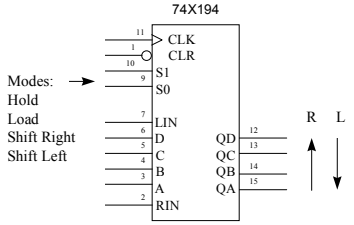


Octal (8-bit) SISO, PISO



MSI Shift Registers

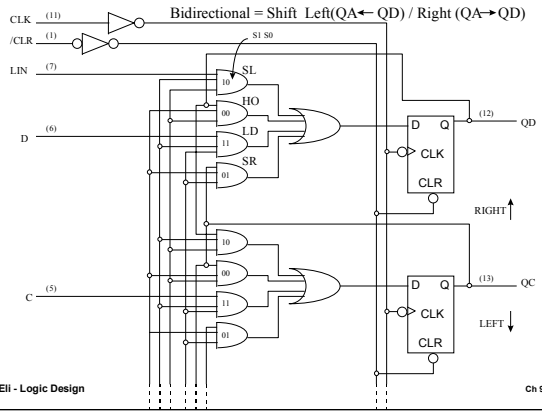
Quad Bidirectional Universal (4-bit) PIPO



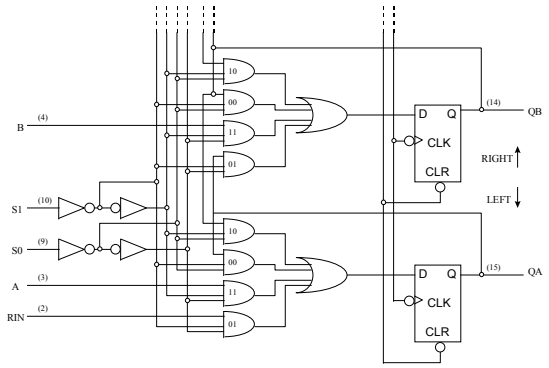
74x194 State table (4 functions)

	Input		Next state			
Function	S1	S0	QA*	QB*	QC*	QD*
Hold	0	0	QA	QB	QC	QD
Shift right	0	1	RIN	QA	QB	QC
Shift left	1	0	QB	QC	QD	LIN
Load	1	1	A	B	C	D

74x194 Schematic

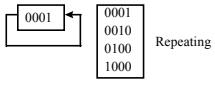


Universal shift register

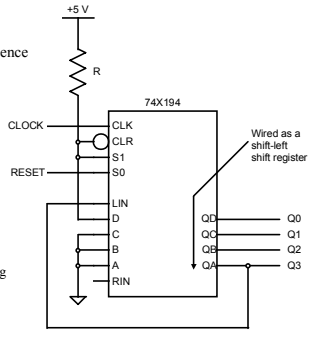


Shift Register Control Application: Ring Counter

- Shift Register Counter
  - cyclic state diagram
  - not normal counting sequence
- Ring Counter
  - n states with n-bit Shift Register
  - simplest form
  - initially reset to load 0001 => Q_{ABCD}



- Glitch-free 1-of-n decoder (Chap.)



Ring Counter Timing